



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,178	01/30/2004	Arya Reza Behzad	BP 2475	7634
51472	7590	01/12/2006	EXAMINER	
GARLICK HARRISON & MARKISON LLP			NGUYEN, KHAI M	
P.O. BOX 160727			ART UNIT	PAPER NUMBER
AUSTIN, TX 78716-0727			2819	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,178	BEHZAD, ARYA REZA <i>(pm)</i>	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 11/10/2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-13, 15 and 16 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-13, 15 and 16 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 1/30/2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

1. The allowability of claims 5-6, 10-11, and 15-16 has been withdrawn.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3, 4, 7-9, 12, and 13 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-3, 6, 4-6, 9-10, and 16, respectively, of U.S. Patent No. 6,496,067. Although the conflicting claims are not identical, they are not patentably distinct from each other because the identified claims of the '067 patent contains similar limitations of the claimed invention (see and compare those claims as identified above).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-13, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Behzad et al. (US 6,496,067).

The applied reference has a common inventor with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention “by another,” or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Behzad et al. discloses (Figs. 5 & 9) a DC coupled class AB transconductance block, comprising:

first DC coupled transconductance stage (12) comprising MOSFET amplification devices (see column 1, line 28; and transistors 42/44 of Fig. 9) operably coupled to produce a first differential current (20) from a differential input voltage (18) based on a first bias voltage (22);

second DC coupled transconductance stage (14) comprising MOSFET amplification devices (46/48) operably coupled to produce a second differential current (24) based on the differential input voltage (18) and a second bias voltage (26), wherein an output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current (output current 28); and biasing circuit (16) operably coupled to produce the first bias voltage and the secondary bias voltage, wherein the first bias voltage is greater than the secondary bias voltage.

Regarding claim 2, Behzad et al. discloses (Figs. 5 & 9) the first transconductance stage (12) further comprises:

first DC coupled transistor (42 or 44) operably coupled to receive a combination of a first leg of the differential input voltage (V_{in+} or V_{in-}) and the first bias voltage (V_{ref}); and

second DC coupled transistor (44 or 42) operably coupled to receive a combination of a second leg of the differential input voltage (V_{in-} or V_{in+}) and the first bias voltage ($V_{ref} -$ bias voltage 22), wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the first differential current and the second transistor produces a second leg of the first differential current.

Regarding claim 3, Behzad et al. discloses (Fig. 10) the second transconductance stage (14) further comprises:

first DC coupled transistor (46 or 48) operably coupled to receive a combination of a first leg of the differential input voltage (Vin+ or Vin-) and the secondary bias voltage (2nd bias voltage 26); and

second DC coupled transistor (48 or 46) operably coupled to receive a combination of a second leg of the differential input voltage (Vin- or Vin+) and the secondary bias voltage (bias voltage 26), wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

Regarding claim 4, Behzad et al. discloses the class AB voltage to current converter of claim 3 further including a third transconductance stage (stage 102 of Fig. 12), the third transconductance stage further comprising:

first DC coupled transistor (42) operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and

second DC coupled transistor (44) operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current (see Figs. 9-11).

Regarding claims 5-6, 10-11, and 15-16, Behzad et al. discloses Fig. 12 comprising the fourth stage and/or the fifth stage of the claimed invention – these stages are configured the same as the first/second stages (column 6, lines 44-51).

Regarding claim 7, Behzad et al. discloses the biasing circuit of claim 1 comprises a reference current source operably coupled to a current mirror (including 112 and current source pair 114) to produce a bias signal (see 112 of Fig. 13).

Regarding claim 8, Behzad et al. discloses (Fig. 10) the biasing circuit of claim 1 comprises:

first reference voltage source (58 or 60) operably coupled to produce the first bias voltage (22);

second reference voltage source (60 or 58) operably coupled to produce the secondary bias voltage (26);

first resistive pair (54/56) operably coupled to provide the first bias voltage to the first transconductance stage; and

second resistive pair (74/76) operably coupled to provide the secondary bias voltage to the secondary transconductance stage.

Regarding claim 9, Behzad et al. discloses (stage 102 of Fig. 12) the class AB voltage to current converter of claim 1 further comprises:

third transconductance stage (102) operably coupled to produce a third differential current (104) based on the differential input voltage (18) and a third bias voltage (106), wherein output current of the class AB voltage current converter is the sum of the first differential current, the second differential current, and the third differential current, wherein the biasing circuit produces the third bias voltage, wherein the second bias voltage is greater than the third bias voltage (the first, second, and third bias voltages are imbalanced – see column 6, lines 65-67).

Regarding claim 12, Behzad et al. discloses (Fig. 10) a DC coupled class AB transconductance block, comprising:

first DC coupled transconductance stage (12) operably coupled to produce a first differential current (20) from a differential input voltage (18) based on a first bias voltage (22);

second DC coupled transconductance stage (14) operably coupled to produce a second differential current (24) based on the differential input voltage (18) and a second bias voltage (26), wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current (28);

biasing circuit (16) operably coupled to produce a bias current;

a resistor ladder (resistor section disposed in the biasing circuit 16) comprising a plurality of resistors (54/56/72/74/76) wherein at least one resistor is electronically coupled between each transconductance stage of the DC coupled class AB transconductance block; wherein the first transconductance stage is biased to a different voltage level relative to the second transconductance stage (column 4, lines 30-40; and Fig. 9); and

wherein an output transconductance signal (28) is a sum of the transconductance signals produced by the first and second of the transconductance stages.

Regarding claim 13, Behzad et al. discloses the DC coupled class AB transconductance block of claim 12 further comprising a third transconductance stage (stage 102 of Fig. 12).

Response to Arguments

4. Applicant's arguments filed 11/10/2005 have been fully considered but they are not persuasive. The applicant argues that the rejection is improper (see page 10). The examiner has reviewed the rejection and confirmed that it is proper because the applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford (Rex) Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Khai M. Nguyen
Art Unit: 2819

571-272-1809